Cyclone V

Application Note

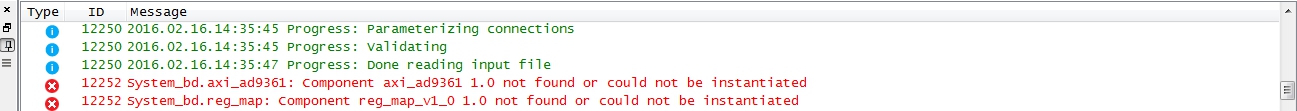
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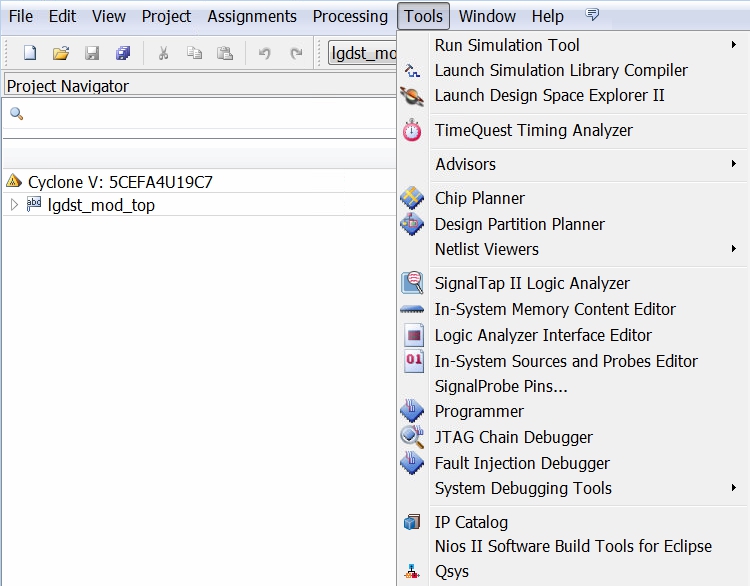
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# QSys Integration

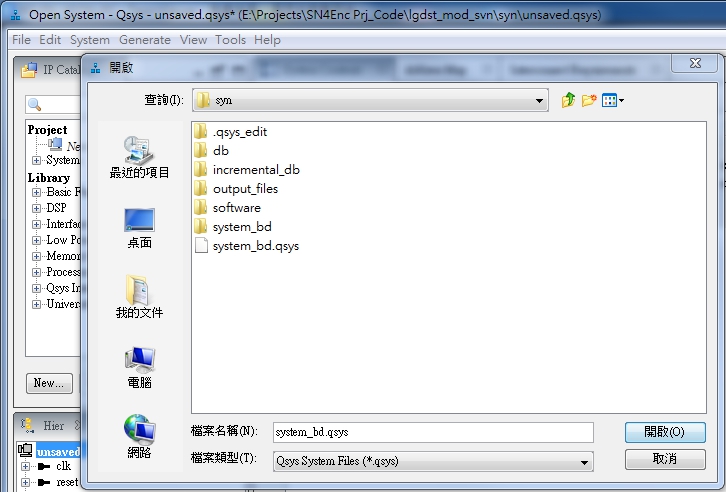
When you saw the error messages in below, it means that you need to set “**IP Search Path**” in QSys.



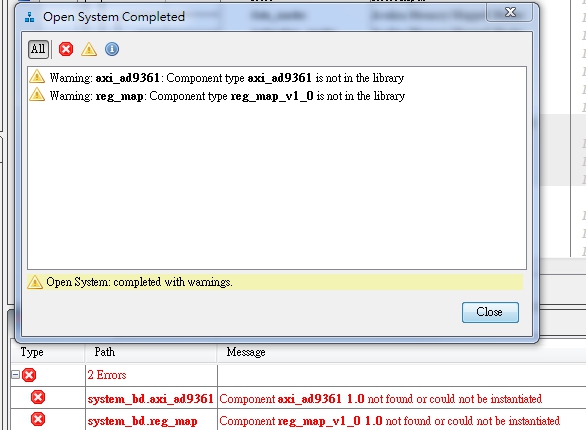
Lunch QSys GUI in Menu **Tools\QSys**



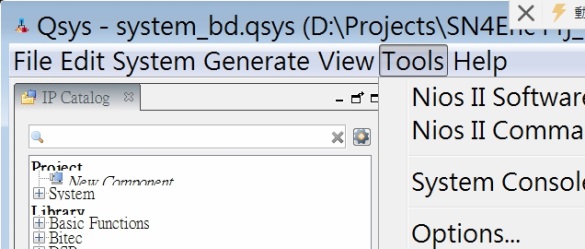
Open QSys file “system\_bd.qsys”



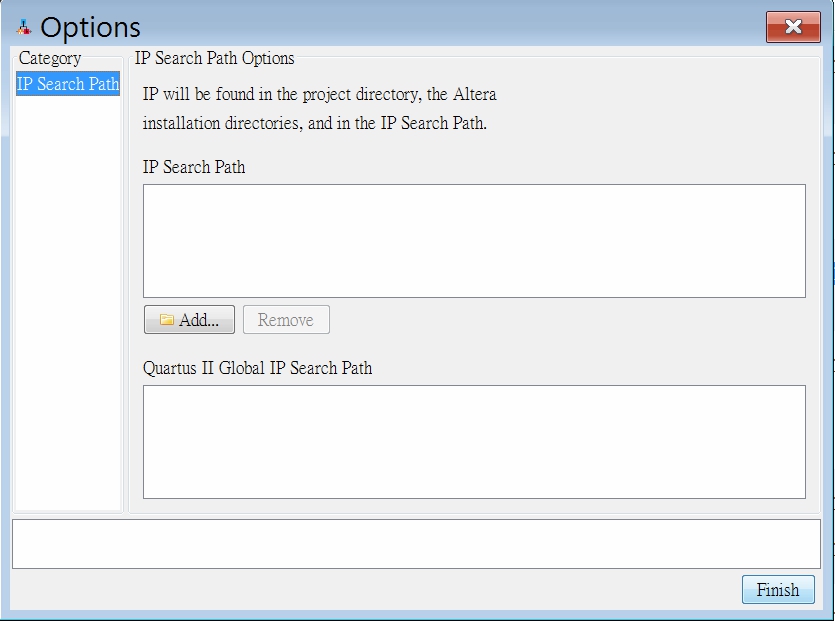
You will see the error messages for missing component ☹



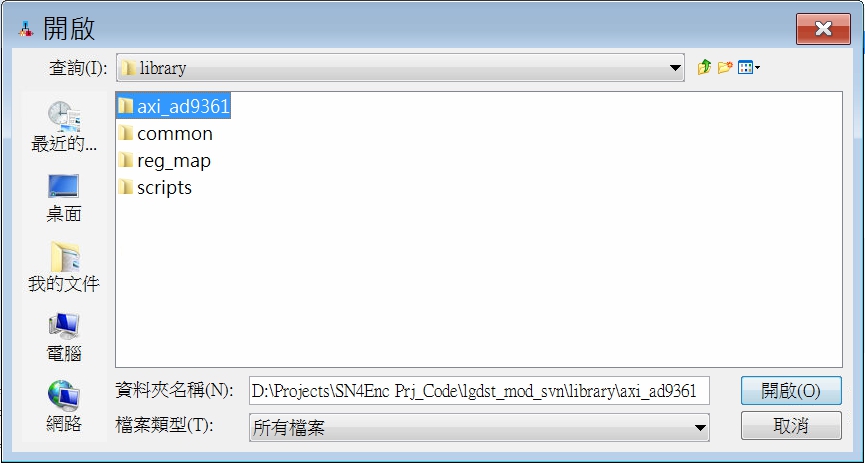
Now start to set the IP Search Path!! Open Setting Dialog in menu **Tools/Options**



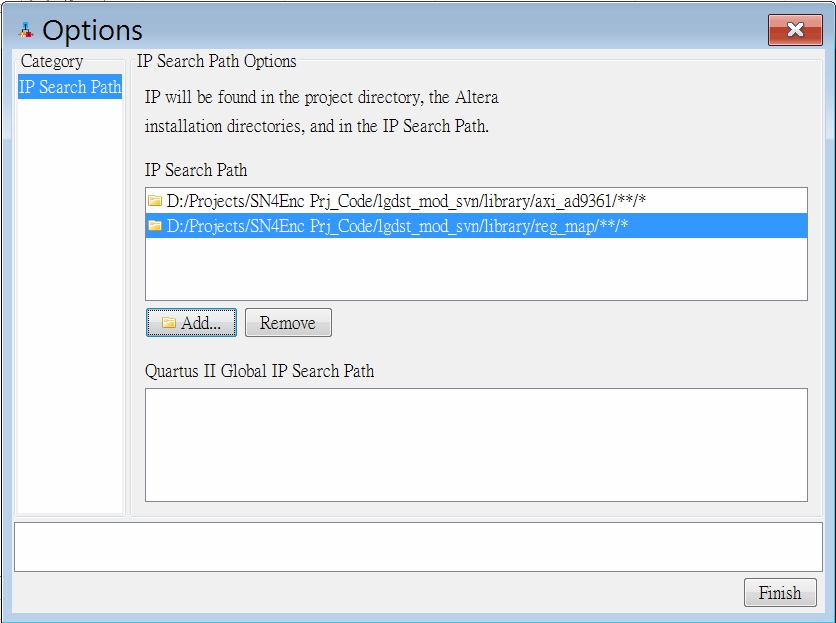
Add two Paths by clicking Add button.



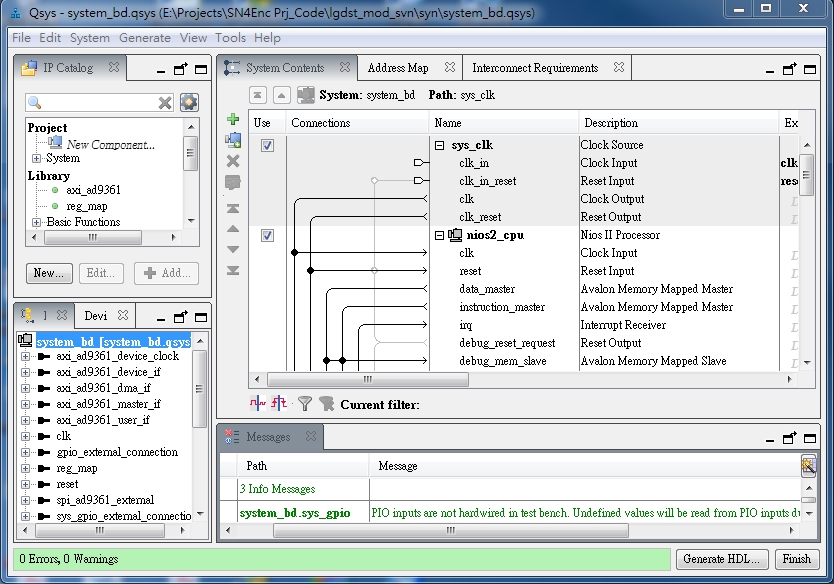
Select the library *axi\_ad9361* and *reg\_map*



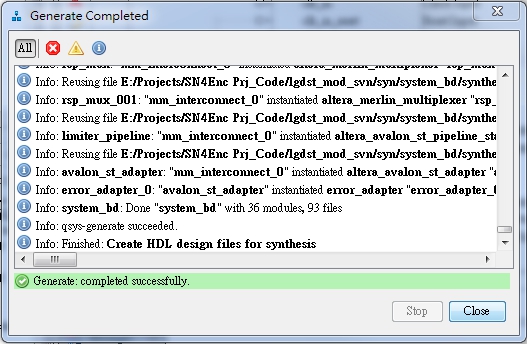
The resulting IP Search Path is as below.



Click “*Generate HDL …*”



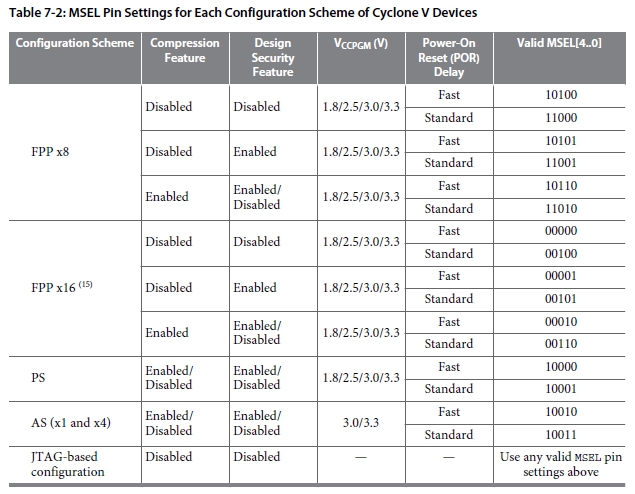
After HDL is generated, Close QSys Tools and restart Fitting.



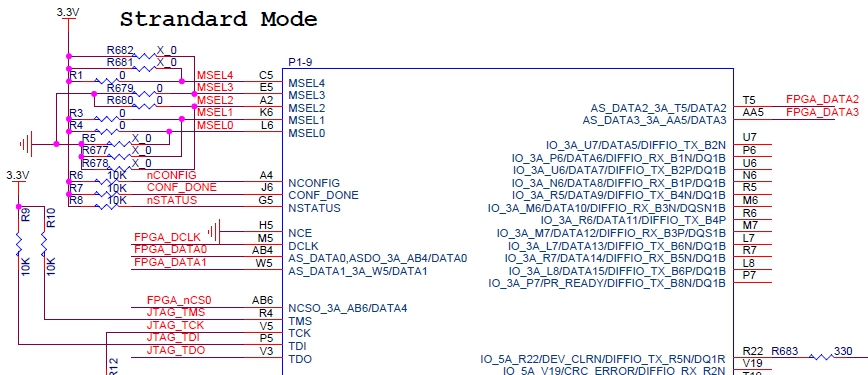
# Instructions for programming Cyclone V PROM

1. Environment Check

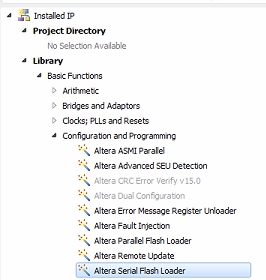
Make sure the Configuration Setting is in AS mode



**lgdst\_mod** pin and assembly setting:



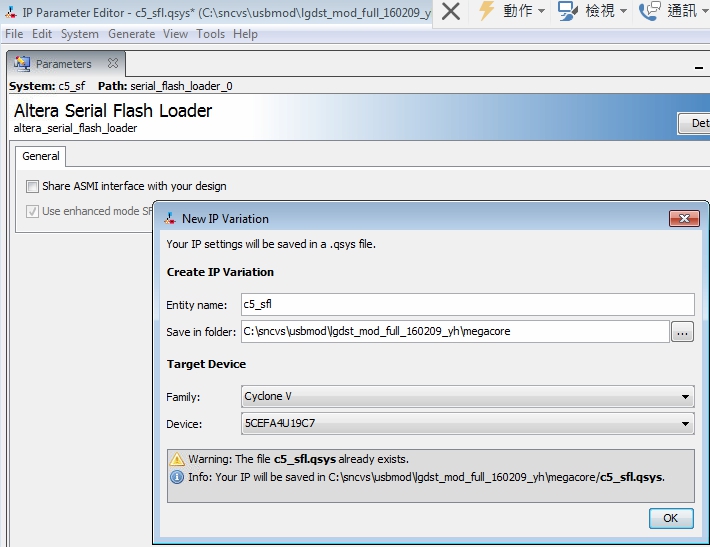
Integrate IP Core “Altera Serial Flash Loader”



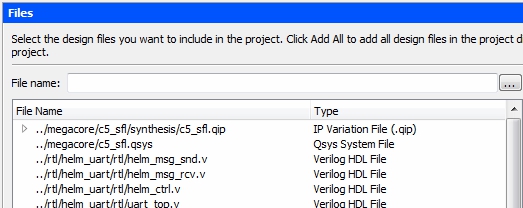
In this example we generate an IP “**named c5\_sfl**”.

DO NOT check “Share ASMI interface with your design” and

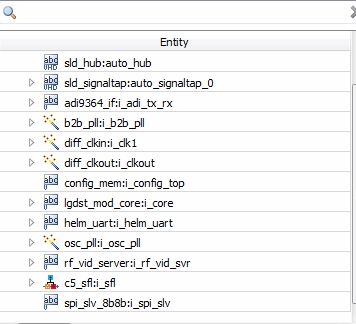
Generate HDL and then finish



Manually add two files into project: c5\_sfl.qip and c5\_sfl\_qsys

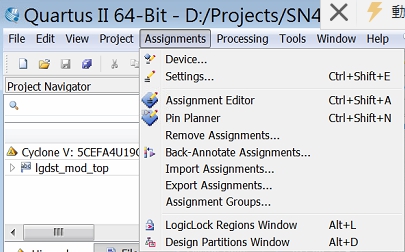


After Fitting you will see the module in Entity List

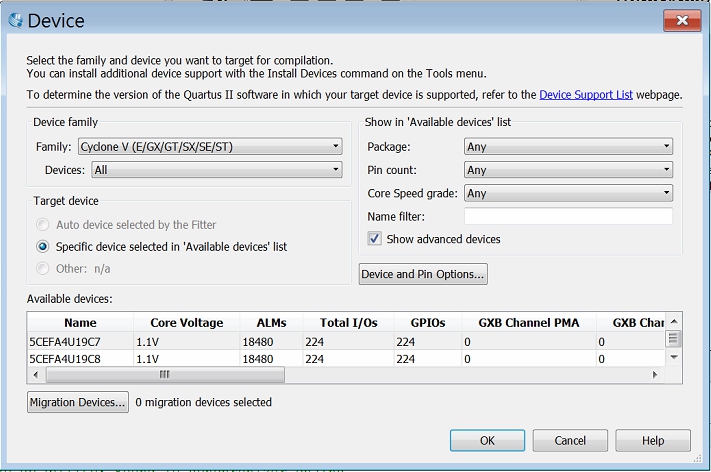


1. Programming Steps
   1. Prepare programming files:

Open Device setting by selecting Assigments/Device…

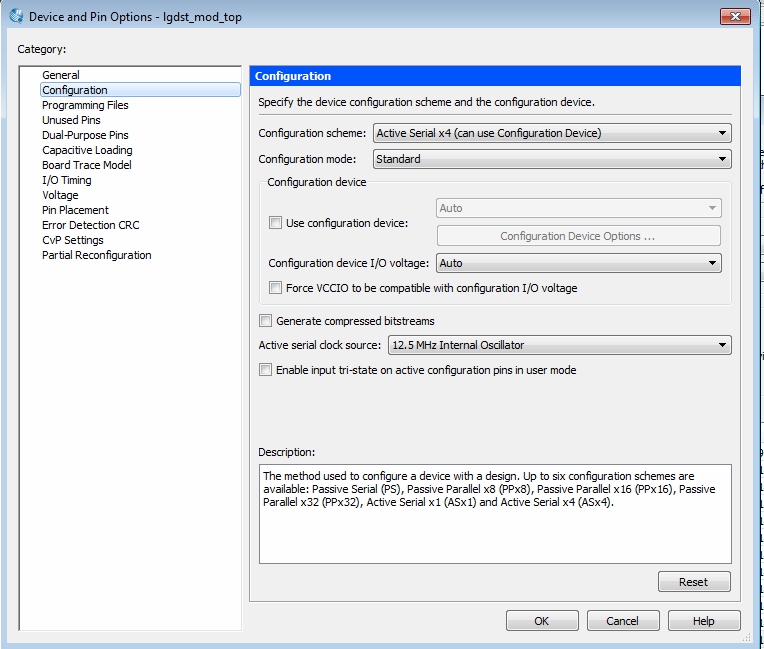


Select the button Device and Pin Options…



Select Configuration Scheme as “Active Serial x4” or “Active Serial x1”

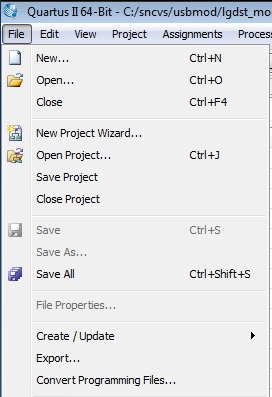
DO Not Check: “Use configuration devices”



*Regenerate the programming file by restart fitting*

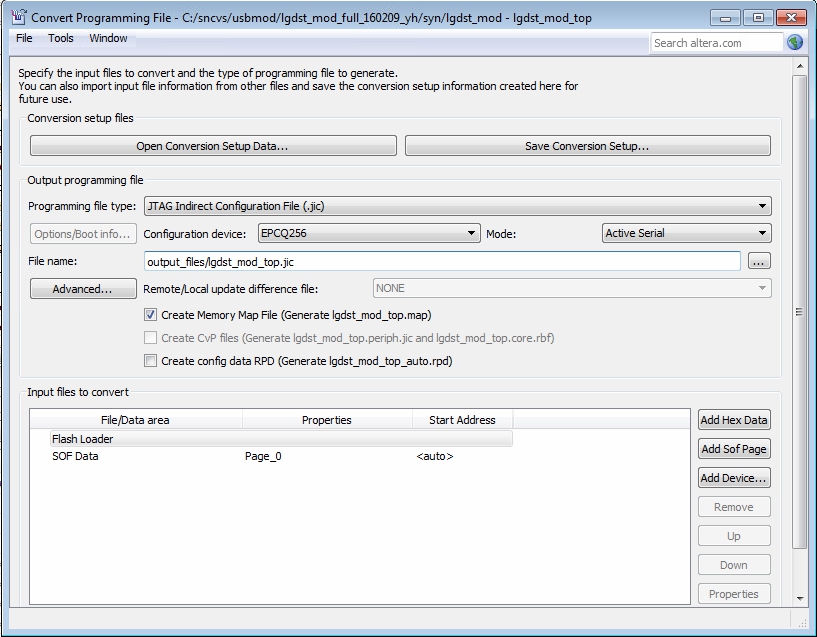
* 1. Convert Programming files

Open Convert Dialog from menu File\Convert Programming Files…

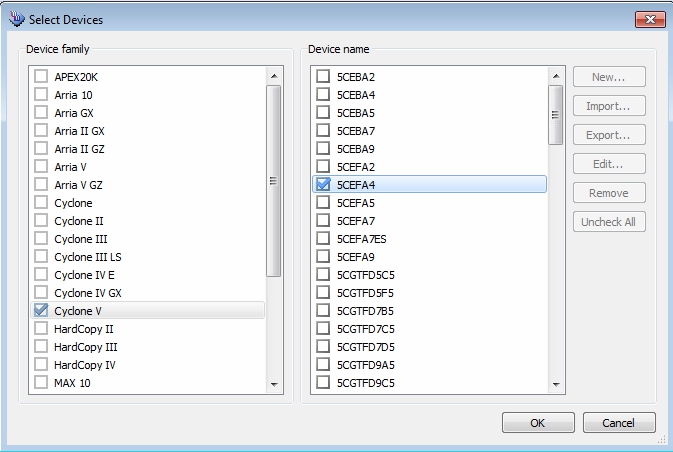


Convert sof file to jic file according the following setting

* Programming file type: JTAG Indiect Configuration File (.jic)
* Configuration device: EPCQ256
* File name: output\_files/filename.jic
* Select Flash Loader and the button “Add Device..” becomes active

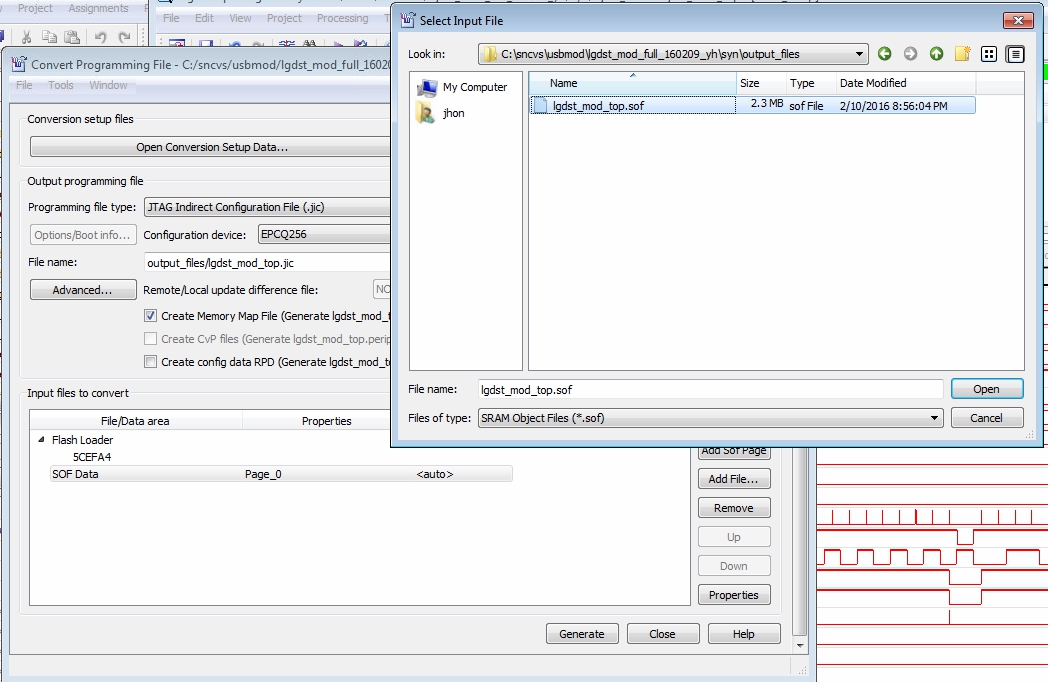


Click button “Add Device…” and selection the FPGA device we used.

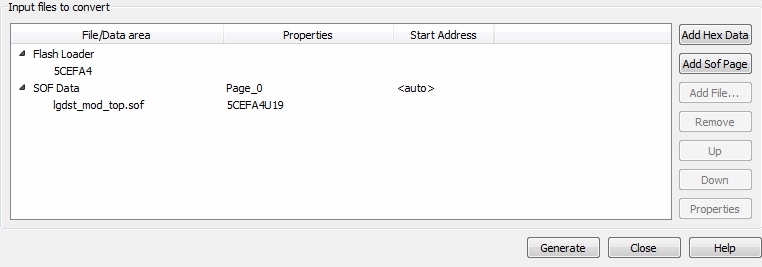


Selection SOF Data and click button “Add File …”

A dialog will popup to select the latest \*.sof file



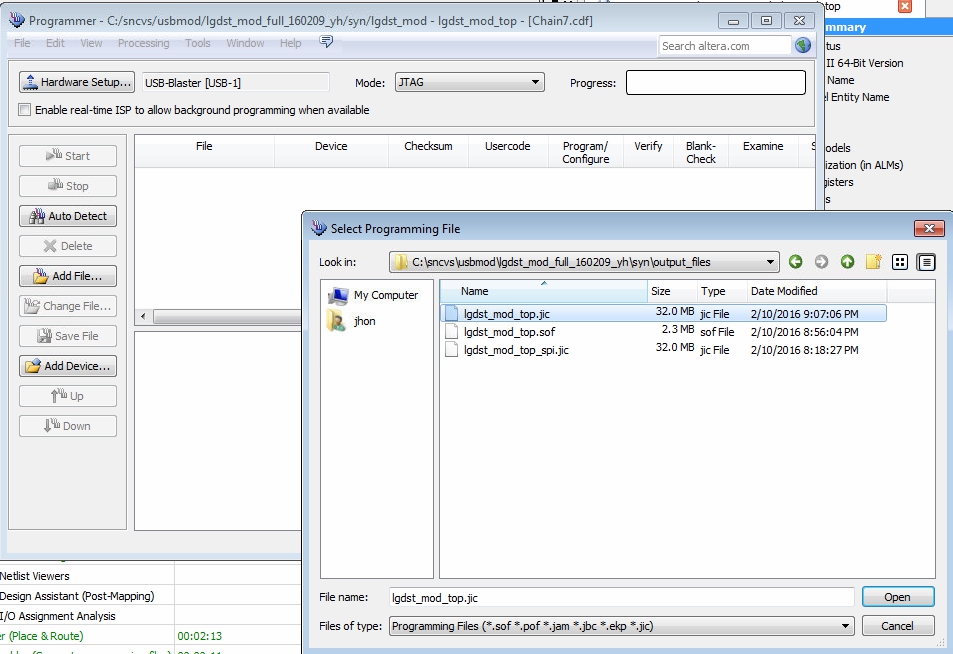
The resulting window is shown as below and press Generate to generate jic file.



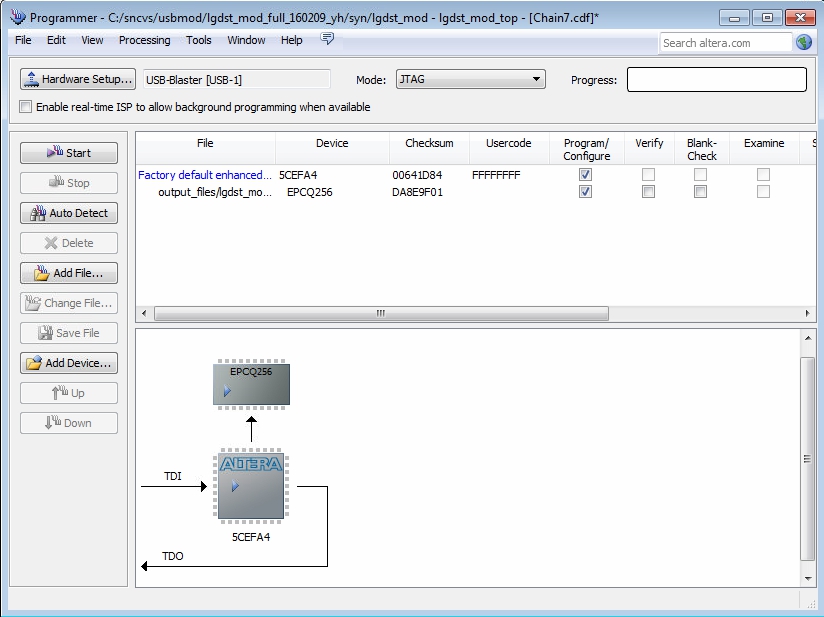
* 1. Programming

Open Programmer and press button “Add File …”

Select the \*.jic file you generated and click OPEN



The Programmer shows as below and check the item Program/Configure



Good luck for your programming!!